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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,201	03/31/2004	Jhon Jhy Liaw	N1280-00180(TSMC2003-1083	9501

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DUANE MORRIS, LLP
IP DEPARTMENT
ONE LIBERTY PLACE
PHILADELPHIA, PA 19103-7396

EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,201	LIAW, JHON JHY	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *26-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election

1. Applicant's election without traverse of Group I, claims 1-25 in the reply filed on 04/15/5 is acknowledged.

2. Claims 26-31 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 04/15/05.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5 and 8-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (U.S. Patent No. 5,187,114) in view of Chan et al. (U.S. Patent No. 5,795,800).

In re claim 1, Chan ('114, Fig. 6) discloses a semiconductor device, comprising:

a first semiconductor device (18) formed on a semiconductor substrate;

a non-conducting gate interconnect layer (30) formed on the semiconductor substrate for connecting to a gate of a second semiconductor device; and

a silicide layer (36) formed on the gate interconnect layer, and an active region of the first semiconductor device for making a connection thereof.

Chan ('114) does not expressly disclose an insulating substrate. Insulating (SOI) substrates are well known in the art as demonstrated by Chan ('800). It would have been obvious for one skilled in the art at the time of the invention to use an SOI underlayer/substrate as disclosed by Chan ('800) for the device of Chan ('114) for the purpose, for example, of minimizing transistor leakage and implantation-induced defects (column 3, lines 36-41).

In re claim 2, Chan ('114) in view of Chan ('800) discloses the device of claim 1, wherein the silicide layer further covers a dielectric edge portion (edge of FOX region 12) separating the gate interconnect layer from the active region.

In re claim 3, Chan ('114) in view of Chan ('800) discloses the device of claim 1, wherein the silicide layer further covers a sidewall of the gate interconnect.

In re claim 4, Chan ('114) in view of Chan ('800) discloses the device of claim 1, wherein the silicon substrate has a thickness of more than 20 angstroms.

In re claim 5, Chan ('114) in view of Chan ('800) discloses the device of claim 1, wherein the active region serves as a local interconnection layer between the first and second semiconductor devices.

In re claims 8 and 15, Chan ('114) discloses an SRAM cell comprising:

at least one active region with a silicide layer formed thereon serving as an intra-cell connection layer connecting drain nodes of at least a PMOS transistor and an NMOS transistor, the two transistors forming a first inverter (column 1, lines 30-32); and

a sidewall butted connection structure used in conjunction with a gate interconnect layer for connecting the drain nodes of the transistors of the first inverter to gates of at least two transistors forming a first inverter.

Chan ('114) does not expressly disclose an insulating substrate. Insulating (SOI) substrates are well known in the art as demonstrated by Chan ('800). It would have been obvious for one skilled in the art at the time of the invention to use an SOI underlayer/substrate as disclosed by Chan ('800) for the device of Chan ('114) for the purpose, for example, of minimizing transistor leakage and implantation-induced defects (column 3, lines 36-41).

In re claims 9 and 22, Chan ('114) in view of Chan ('800) discloses the devices of claims 8 and 15 respectively, wherein the active region further connects to a source node of at least one pass gate (as shown in Figs. 1, 2).

In re claim 10, Chan ('114) in view of Chan ('800) discloses the device of claim 9, wherein the pass gate's drain node is connected to an access line (40, 46).

In re claims 11-14, 16, 18-20 and 23-25, Chan ('114) in view of Chan ('800) discloses the devices of claims 8 and 15 respectively, wherein the device discloses the lines (40 and 46) extending externally from the substrate. The various labels to the external lines such as "power supply", "access" and "landing pads" simply describe intended uses for the lines and do not further limit the structure of the device. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 17, Chan ('114) in view of Chan ('800) discloses the device of claim 15, wherein the first metal layer is also used for forming a connection between the drain nodes (22) of the two transistors of the first or second inverter.

In re claim 21, Chan ('114) in view of Chan ('800) discloses the device of claim 15, further comprising at least one active region (22) with a silicide layer (36) formed thereon serving as an intra-cell connection layer connecting drain nodes of the transistors of the first inverter.

5. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan ('114)/Chan ('800) as applied to claim 1 above, and further in view of Chan (U.S. Patent No. 4,569,112).

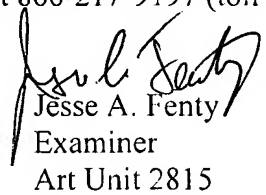
In re claim 6, Chan ('114) in view of Chan ('800) discloses the device of claim 1, but does not expressly disclose the thickness of the silicide layer. Chan discloses the thickness of a connection silicide layer (50) to be in the range of 0.1 microns, about 1000 angstroms (Appendix I). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a thinner silicide layer since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. Since Chan's disclosure was from at least twenty years ago, it would have been within the skill of one in the art to use a thinner silicide layer because semiconductor devices and materials have been scaled down considerably since that time.

In re claim 7, Chan ('114) in view of Chan ('800) discloses the device of claim 1, but does not expressly disclose the resistivity of the silicide layer. Such resistivity is disclosed in the prior art by Chan ('112), Appendix I, being at a level of 5 ohm/ea, within the claimed range.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jesse A. Fenty
Examiner
Art Unit 2815